Description

S6269S is highly integrated current mode PWM control IC for flyback convertor. The maximum output power is up to 80W. S6269S can meet level 6 energy-efficiency standard and EMC requirement easily.
S6269S has comprehensive protection feature to ensure the reliability of system. The packaging form of S6269S has SOP-8.

Features

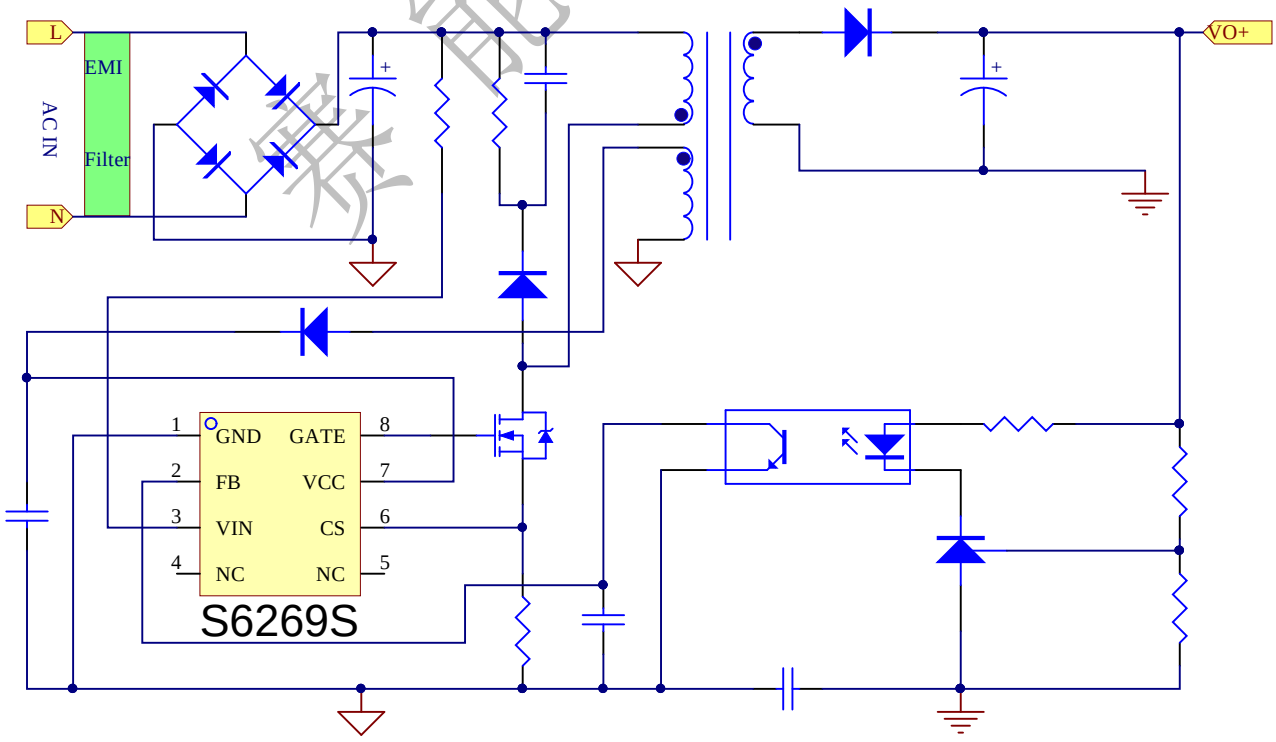
- ⌘ Digit frequency shuffling technology to improve EMI performance.
- ⌘ Fixed 65kHz PWM switching frequency.
- ⌘ Leading-edge blanking on current sense.
- ⌘ Internal synchronized slope compensation.
- ⌘ Low standby power consumption (<75mW@AC 230V)
- ⌘ Soft-start to reduce MOSFET Vds stress during power on
- ⌘ Comprehensive protection function
  1、Under voltage locked with hysteresis (UVLO) on VDD.
  2、Over voltage protection (OVP) on VDD.
  3、Cycle-by-Cycle current limitation.
  4、Over load protection (OLP)
  5、Over temperature protection (OTP)
  6、Current limitation compensation to obtain the same output current in universal ac line input
- ⌘ Low start-up current (<10uA@VDD=12V)
- ⌘ 300mA of sinking and 150mA of sourcing current capability in GATE pin

Applications

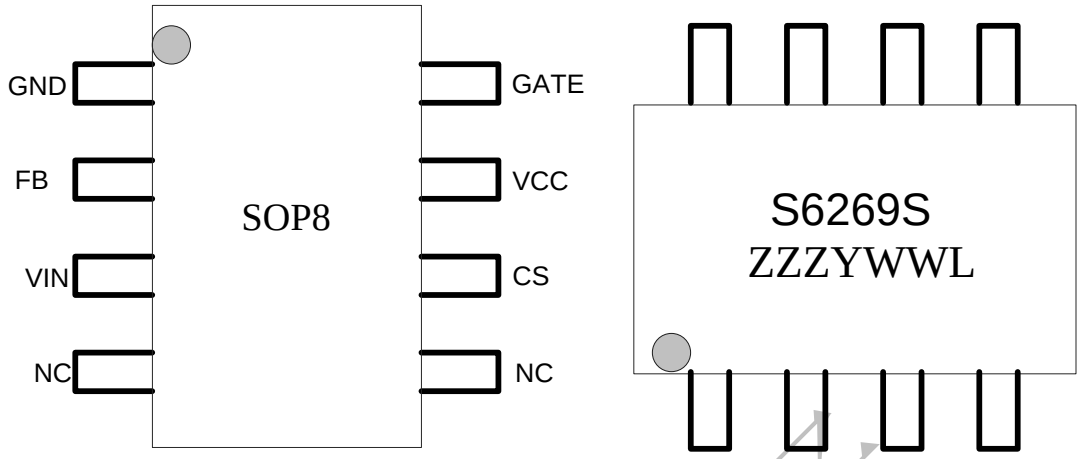
- ⌘ Cell Phone Charger
- ⌘ Digital Cameras Charger
- ⌘ Battery charger

Application Circuit

Two large value resistors are connected to VCC capacitor in startup circuit .



Pin Assignment & Marking Information



ZZZ:	LOT NO
Y:	Year code (2021=A ,2022=B,2023=C,.....)
WW:	week code (01-52)
L:	FAB code

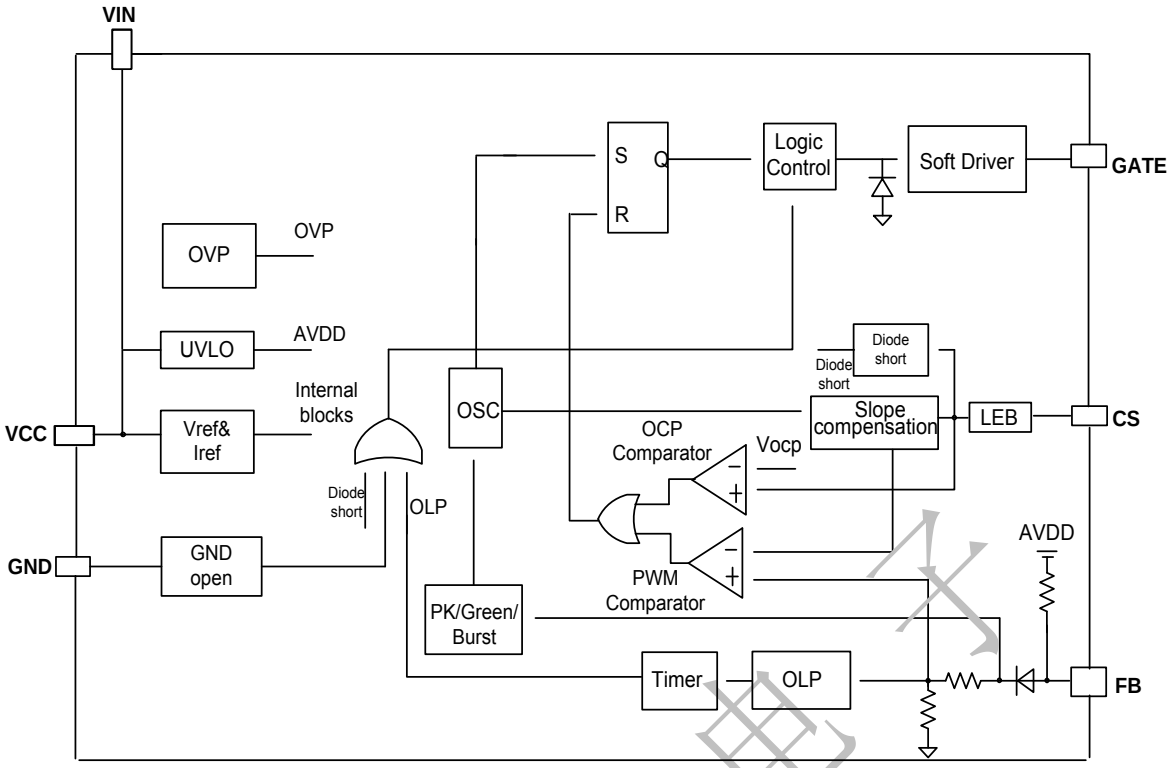
Ordering Information

Part number	Package	MOQ
S6269S	SOP-8	4000pcs

Pin Description

Pin Number	Symbol	Description
1	GND	Ground.
2	FB	Feedback input pin.
3	VIN	Start-up pin
4	NC	NC
5	NC	NC
6	SENSE	Current sense input pin.
7	VDD	Chip DC power supply pin.
8	GATE	Totem-pole gate diver.

Block Diagram



Absolute Maximum Rating

Parameter	Value	Unit
VDD clamp voltage	44	V
VDD clamp current	10	mA
VFB input voltage	-0.3 to7	V
VSENSE input voltage to SENSE pin	-0.3 to7	V
Min/Max operating junction temperature	-55 to 150	℃
Operating ambient temperature	-20 to 85	℃
Thermal resistance, Junction to ambient SOP-8	250	℃/W

Note: Stresses above absolute maximum ratings may cause permanents damage to the device. Exposure to absolutely maximum-rated conditions for extended periods may affects device reliability

Recommended Operating Conditions

Symbol	Parameter	Min. Max.	Unit
VDD	Supply Voltage Vcc	9 to 41	V
Toa	Operating Ambient temperature	-20 to 85	℃
ESD-HM	Human Model	2	KV
ESD-MM	Machine Model	150	V

Electrical Characteristics (T_A = 25 ℃, if not otherwise noted)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Supply Voltage (V_{dd} Pin)						
Idd_start-up	VDD start-up current	VDD=12.5V		3	10	uA
Idd	VDD Operation current	VDD=16V，FB=2V		1.5		mA
UVLO(ON)	VDD under voltage lockout enter		6.8	7.8	9	V
UVLO(OFF)	VDD under voltage lockout exit		12.5	13.5	14.5	V
OVP	VDD over voltage protection		41		43	V
Voltage Feedback (FB Pin)						
AVCS	PWM input gain	VFB/VSENSE		2		V/V
VFB_open	VFB open loop voltage			5.7		V
IFB_short	FB pin short current	Short FB pin to GND		380		uA
VFB_burst	Burst mode voltage			1.0		V
VTH_PL	Power limiting FB threshold voltage			3.7		V
TD_PL	Power limiting delay time			60		mS
DC_MAX	Maximum duty cycl	VDD=18V, SENSE=0V FB=2.2V		75		%
Current Sensing (SENSE Pin)						
T_blanking	Leading-edge blanking time		100	310	600	nS
ZSENSE_IN	Input impedance			40		KΩ
VTH_sense	Over current threshold voltage	Duty=0%		0.7		V
Oscillator						
Fosc	Normal oscillation frequency			65		KHz
Δf_temp	Frequency temperature stability	TA= -20℃ to 100℃		5		%
f_VDD	Frequency voltage stability	VDD=16.5V to 25V		5		%
Fosc_BM	Burst mode base frequency		17	25	28	KHz
Δf_OSC	Frequency modulation range Base frequency		-5		+5	%
Gate Drive Output						
VOL	Output low level	VDD=16V, IO=-20mA			0.8	V
VOH	Output high level	VDD=16V, IO=20mA	10			V
V_Clamp	output clamp voltage level			12		V
T_r	Output rising time	VDD=16V, CL=1nF		680		nS
T_f	Output falling time	VDD=16V, CL=1nF		40		nS

Application Information

S6269S is a highly integrated PWM control IC for the flyback converter. S6269S is designed specifically for switching power supply that requires level 6 energy-efficiency. The input power is less than 75mW at No-load condition in universal input voltage rang.

Start up Control

S6269S has very low start-up current that is less than 10uA. Therefore, a large resistor can be used in start-up circuit of switch power supply. This will minimize standby dissipation. The typical resistance of start-up resistor is 4M ohms.

Operating Current

The Operating current of S6269S is less than 1.5mA. Therefore, S6269S can have good efficiency.

Frequency shuffling for EMI improvement

The frequency Shuffling is implemented in S6269S. The oscillation frequency is modulated with a random source so that the harmonic energy is spread out. The spread spectrum minimizes the conduction EMI and therefore reduces system design challenge.

Burst Mode Operation

At zero load or light load condition, the main power dissipation in a switching mode power supply is from switching on the MOSFET, the core of transformer and the snubber circuit. The magnitude of power dissipation is proportional to the number of switching frequency within certain period. Less switching frequency can reduce the power dissipation. S6269S adjusts the switching frequency according to the loading condition. The PWM pulse width is kept greater than 1.2uS at any load condition. From light load to no load, the FB voltage drops. While the FB voltage is less than 1.1V, the gate pin output is disabled and kept low, while the FB voltage is higher than 1.2V, the gate output recovers to normal working mode. This is called ‘burst mode’. To reduce audio noise, the switching frequency will be kept higher than 20KHz in burst mode.

Oscillator Operation

The switching frequency is internally fixed at 65kHz. No external frequency setting components are required on PCB design.

Current Sensing and Leading-Edge Blanking

Cycle-by-Cycle current limitation is offered in S6269S. The switching current is detected by a resistor into the SENSE pin. An internal leading-edge blanking circuit chops off the SENSE voltage spike at initial so that the external RC filtering on SENSE pin is no longer required. The current limiting comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the voltage in the SENSE pin and the FB pin.

Internal Synchronized Slope Compensation

Slope compensation circuit adds voltage ramp onto the SENSE voltage according to PWM pulse width. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage. Slope compensation can help S6269S obtain the same output current in universal ac input voltage.

Gate Drive

The GATE pin of S6269S has 300mA of sinking and 150mA of sourcing current capability. Therefore, the MOSFET would be turned on slowly and turned off fast so that S6269S has high efficiency and low radiation EMI. The highest voltage of drive voltage is clamped at 12V.

Protection Controls

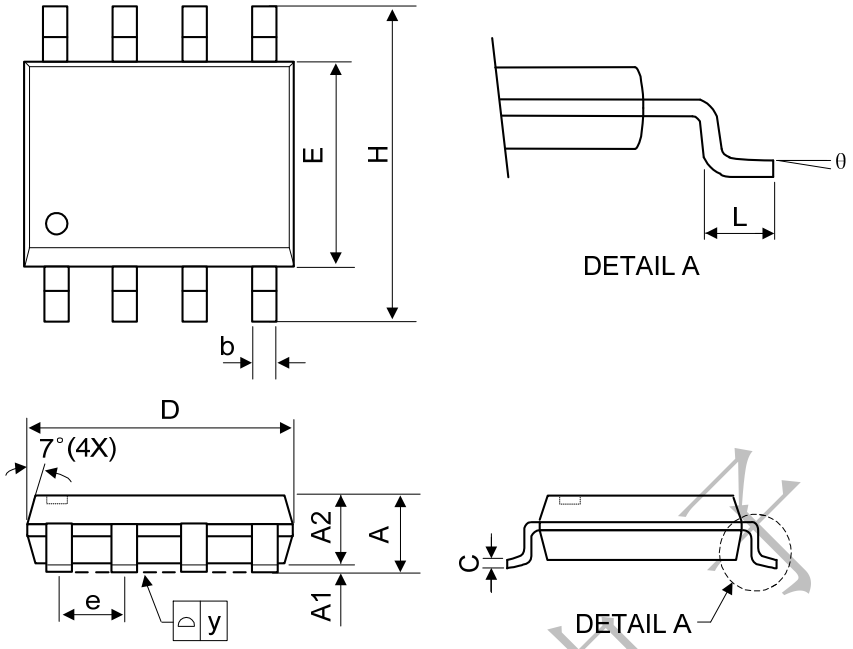
S6269S has comprehensive protection functions, including Cycle-by- Cycle current limitation (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP).

Current limitation compensation

To obtain the same output current capability, the OLP threshold voltage is compensated for the different input AC voltage. This function makes the current of OLP is in consistency whatever the AC input is (110V or 220V).

Package Information

SOP-8



SYMBOL	MILLIMETER			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.04	-	0.1
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
θ	0^O	-	8^O	0^O	-	8^O